



my_and_2.vhd

my_or_2.vhd

- library IEEE;
- use IEEE.STD_LOGIC_1164.ALL;
- use IEEE.STD_LOGIC_ARITH.ALL;
- use IEEE.STD_LOGIC_UNSIGNED.ALL;
- -- Uncomment the following lines to use the declarations that are
- -- provided for instantiating Xilinx primitive components.
- --library UNISIM;
- --use UNISIM.VComponents.all;
- entity my_and_2 is
- port (i1, i2: in std_logic;
- o1: out std_logic);
- end my_and_2;
- architecture Behavioral of my_and_2 is
- begin
- o1 <=i1 and i2;
- end Behavioral;

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- -- Uncomment the following lines to use the declarations that are
- -- provided for instantiating Xilinx primitive components.
- --library UNISIM;
- --use UNISIM.VComponents.all;
- entity my_or_2 is
- Port (i1 : in std_logic;
- i2 : in std_logic;
- o1 : out std_logic);
- end my_or_2;
- architecture Behavioral of my_or_2 is
- begin
- o1 <=i1 or i2;
- end Behavioral;